Amendments to the Claims:

The following listing of claims will replace all prior versions, and listings, of claims in the application:

1. Canceled.

2. (Currently Amended) A semiconductor device including a bonding pad, wherein the bonding pad is a multiple wiring layer structure, the bonding pad comprising:

a first conductive layer connected to a conductive member for external connection;

a second conductive layer disposed below said first conductive layer, the second conductive layer having a plurality of openings ~~and~~ forming a planar ~~network~~ lattice conductive pattern;

a third conductive layer disposed below said second conductive layer, wherein said plurality of openings are sandwiched between the first and third conductive layers;

a first insulating interlayer disposed between said first conductive layer and said second conductive layer;

at least one first through hole provided in said first insulating interlayer;

a fourth conductive layer filling said at least one first through hole;

a second insulating interlayer disposed between said second conductive layer and said third conductive layer;

at least one second through hole provided in said second insulating interlayer wherein said at least one first through hole is disposed substantially directly above said at least one second through hole; and

a fifth conductive layer filling said at least one second through hole, wherein said first insulating interlayer and said second insulating interlayer are connected to each other through said openings of said second conductive layer, and a contiguous section of s

first insulating interlayer with said second insulating interlayer is, thereby, formed between said first conductive layer and said third conductive layer.

3. Canceled

4. (Withdrawn-Currently Amended) A semiconductor device having a multiple wiring layer structure, comprising:

a first conductive layer connected to a conductive member for external connection;

a second conductive layer disposed below said first conductive layer the second conductive layer having a plurality of openings forming a planar lattice conductive pattern;

a third conductive layer disposed below said second conductive layer;

a first insulating interlayer disposed between said first conductive layer and said second conductive layer;

a first through hole provided in said first insulating interlayer;

a fourth conductive layer filling said first through hole;

a second insulating interlayer disposed between said second conductive layer and said third conductive layer;

a second through hole provided in said second insulating interlayer; and

a fifth conductive layer filling said second through hole, wherein said first insulating interlayer and said second insulating interlayer are connected to each other through said openings of said second conductive layer, and a contiguous section of said first insulating interlayer with said second insulating interlayer is, thereby, formed between said first conductive layer and said third conductive layer, said third conductive layer is the lowest conductive layer formed on an insulating film covering a surface of a semiconductor substrate, and said third conductive layer is also provided with a plurality of openings.

5. (Withdrawn-Currently Amended) The semiconductor device according to claim 4, wherein said third conductive layer has a planar ~~network~~ lattice conductive pattern.

6. (Previously Presented) The semiconductor device according to claim 2, wherein said conductive member for external connection is a bonding wire.

7. (Withdrawn) The semiconductor device according to claim 2, wherein said first conductive layer, said second conductive layer and said third conductive layer comprise aluminum as a major component, and said fourth conductive layer and said fifth conductive layer comprise tungsten as a major component.

8. (Withdrawn) The semiconductor device according to claim 2, wherein said semiconductor device further comprises an internal circuit, said internal circuit being formed by the multiple wiring layer structure, and said first conductive layer, said second conductive layer, said third conductive layer, said fourth conductive layer, said fifth conductive layer, said first insulating interlayer, said second insulating interlayer, said through holes, and said multiple wiring layer structure are formed by a collective production process.

9-11. Canceled.

12. (Previously Presented) The semiconductor device according to claim 2, wherein the first and second through holes are axially aligned.

13. (Withdrawn) The semiconductor device according to claim 2, wherein the first and second through holes are axially offset.

14. (Withdrawn) The semiconductor device according to claim 2, wherein the fourth and fifth conductive layers do not overlap.

15-20. Canceled.

21. (Withdrawn) The semiconductor device according to claim 4, wherein the contiguous section is formed perpendicularly between said first conductive layer and said third conductive layer.